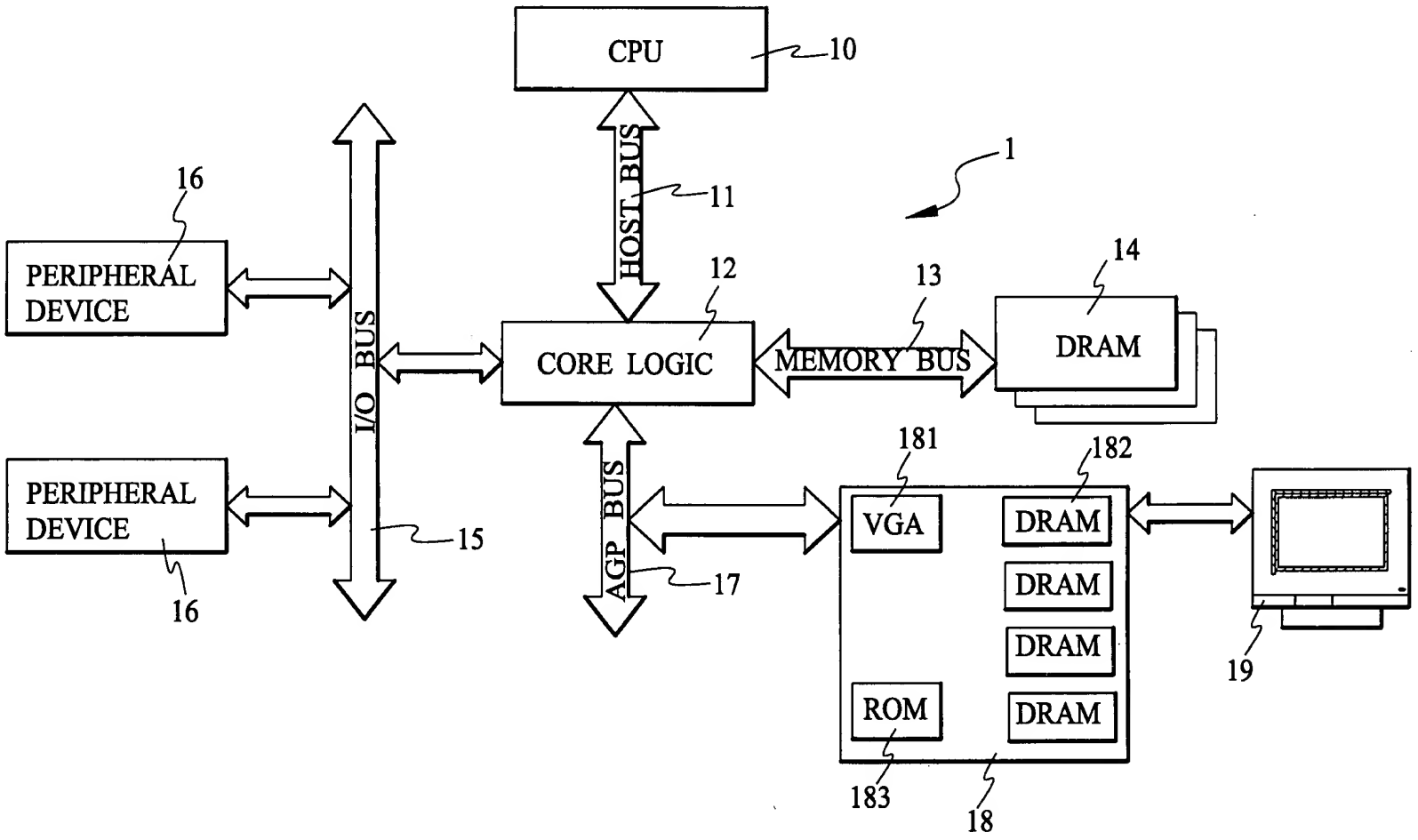

FIG.1 PRIOR ART

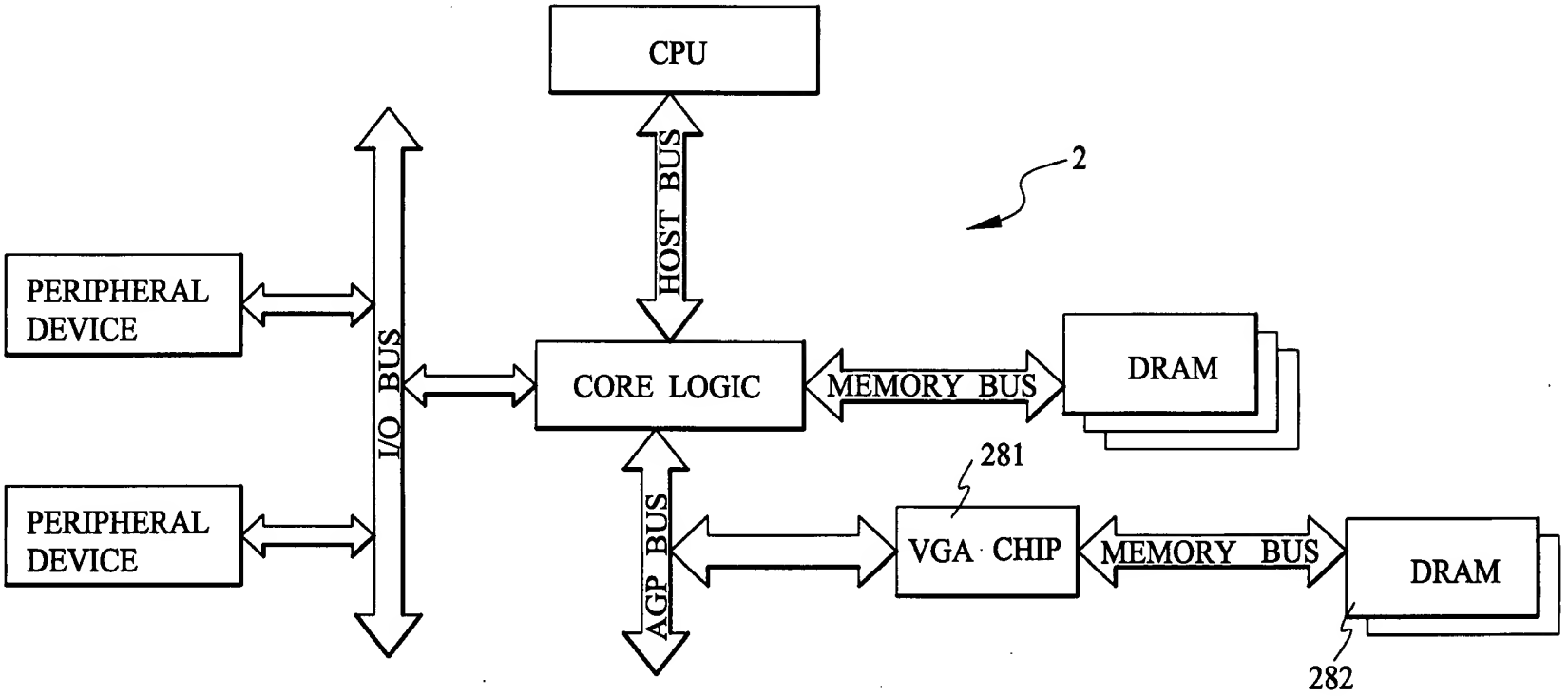

FIG.2 PRIOR ART

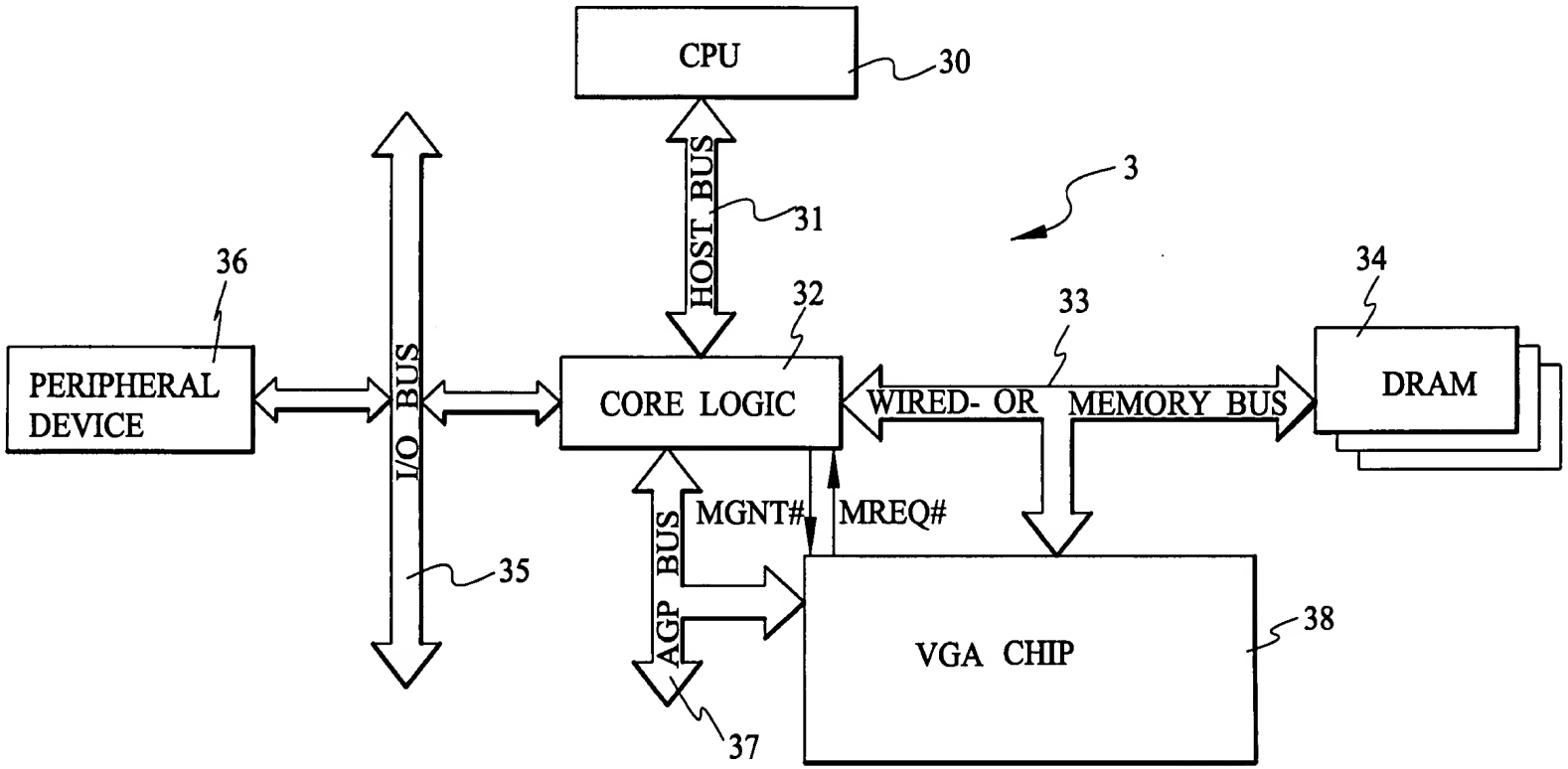

FIG.3 PRIOR ART

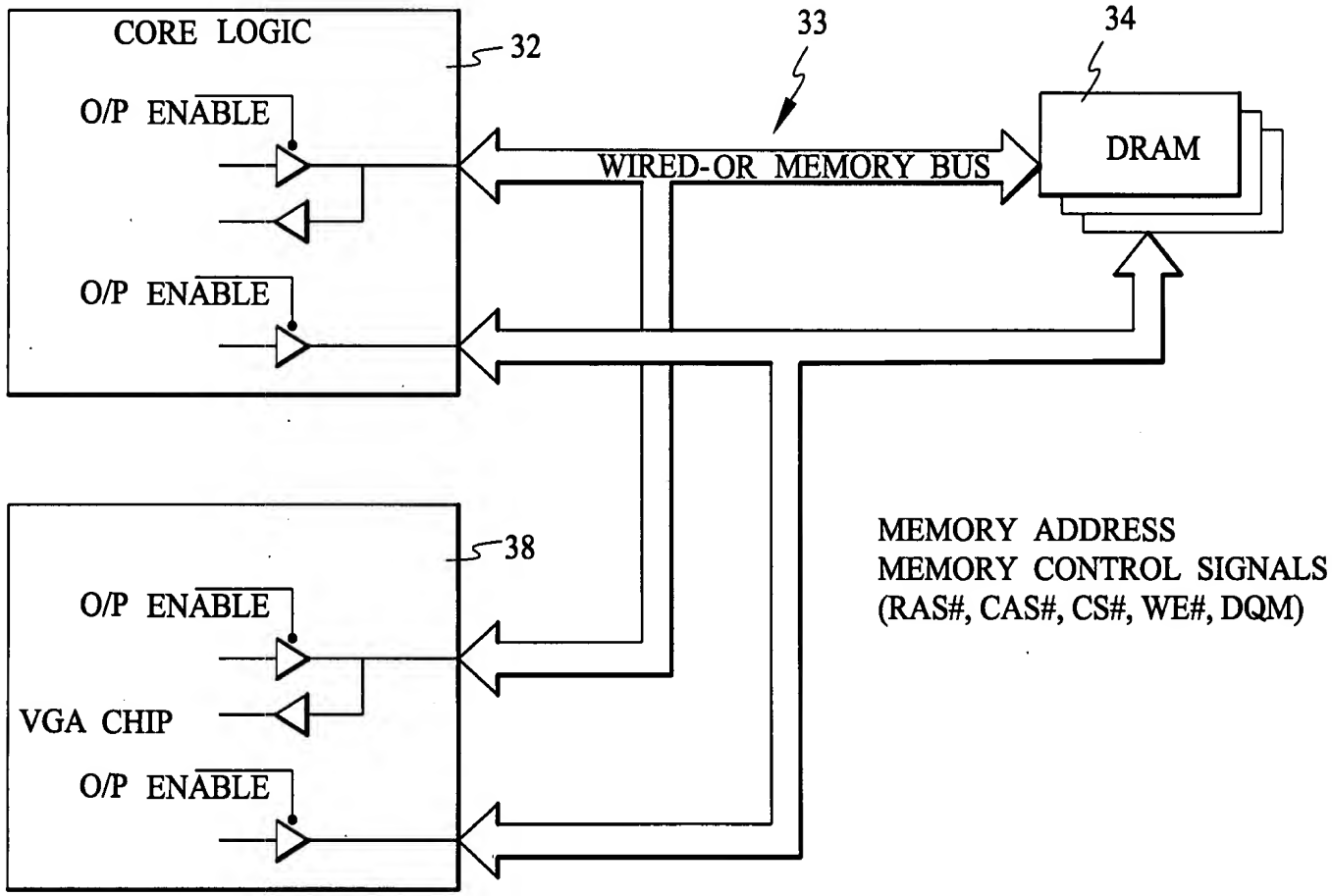

FIG.4 PRIOR ART

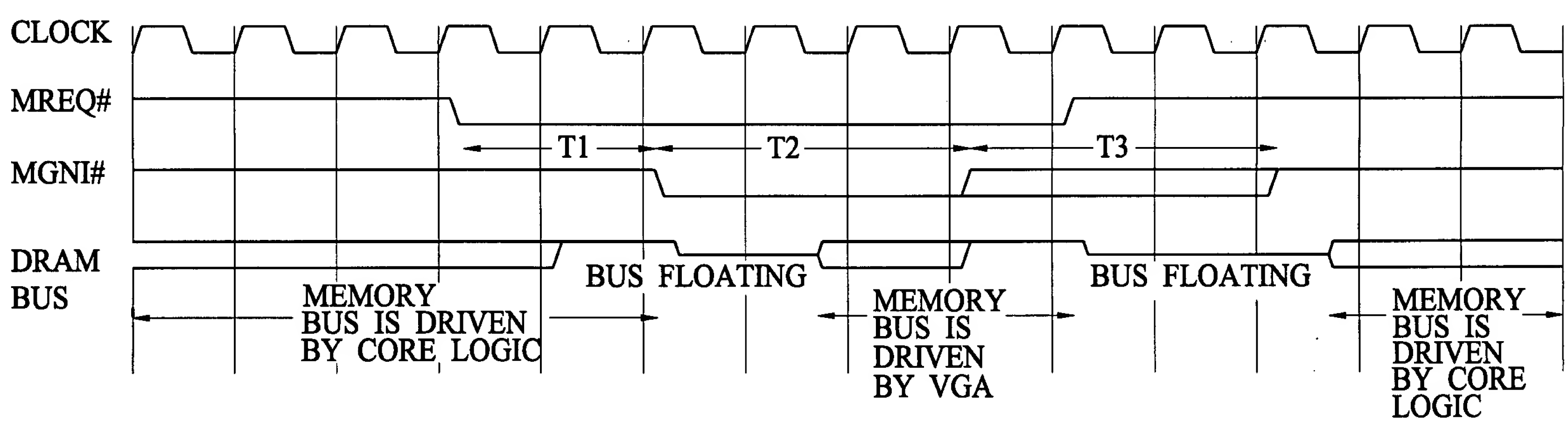

FIG.5 PRIOR ART

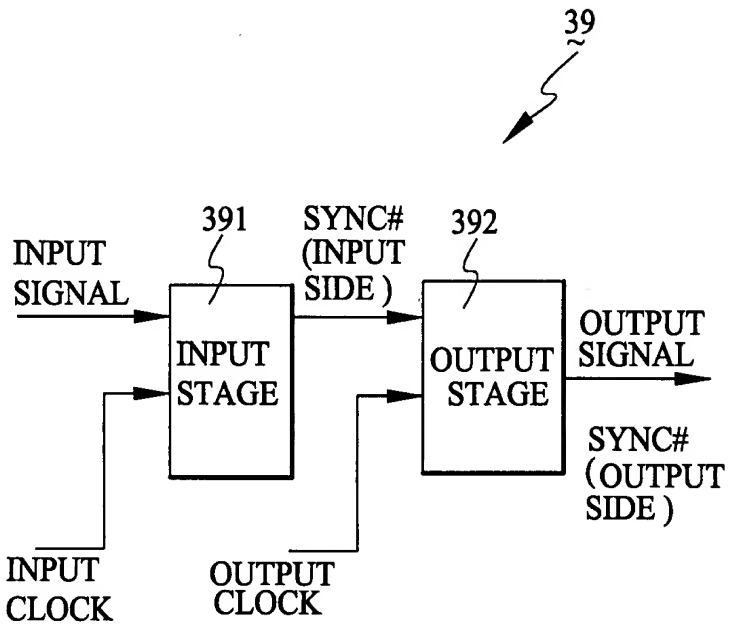

FIG.6 PRIOR ART

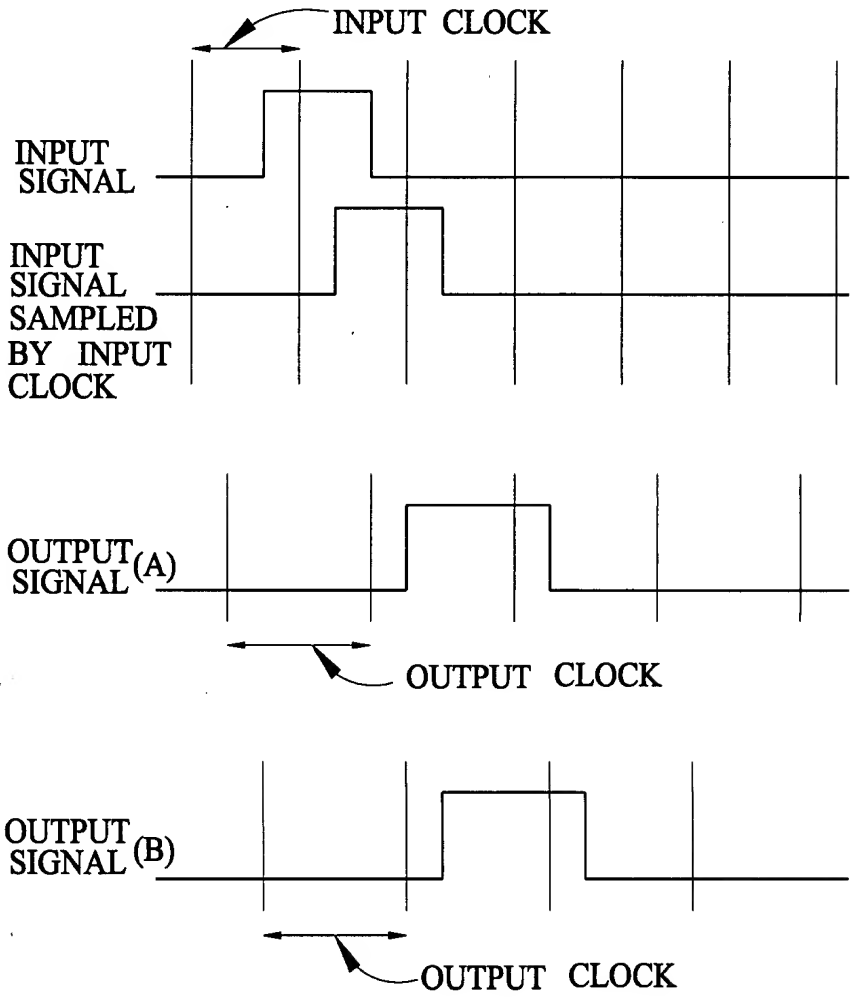

FIG.7 PRIOR ART

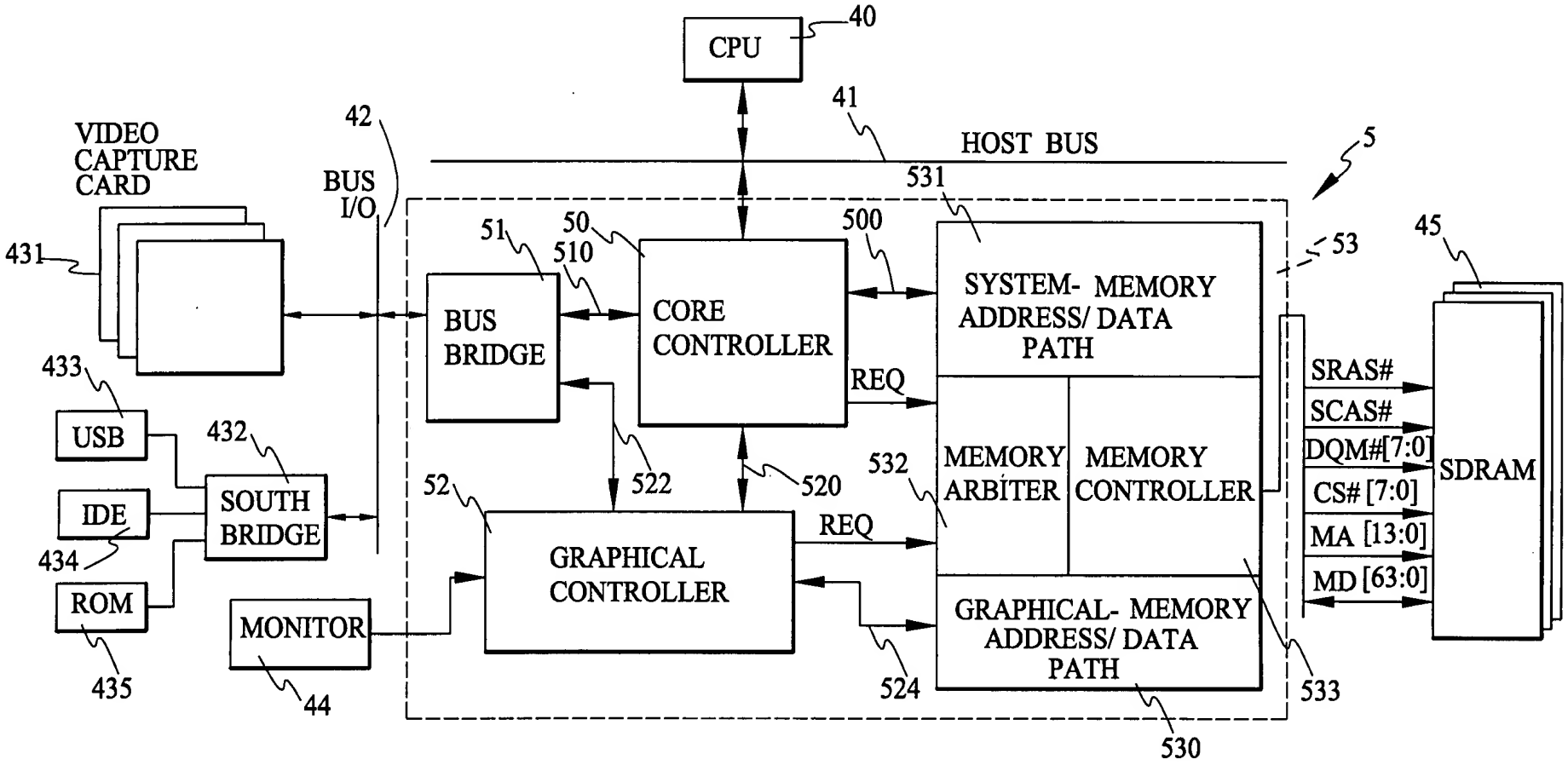
CPU
40
41
HOST BUS
42
BUS I/O
VIDEO CAPTURE CARD
431
5
531
500
50
51
510
53
45
BUS BRIDGE
CORE CONTROLLER
SYSTEM- MEMORY ADDRESS/ DATA PATH
REQ
SRAS#
SCAS#
DQM#[7:0]
CS# [7:0]
MA [13:0]
MD [63:0]
SDRAM
433
USB
432
IDE
SOUTH BRIDGE
434
ROM
435
MONITOR
44
52
522
520
532
MEMORY ARBITER
MEMORY CONTROLLER
REQ
GRAPHICAL CONTROLLER
GRAPHICAL- MEMORY ADDRESS/ DATA PATH
524
533
530

FIG.8